ANALOG SIGNAL CONDITIONING DESIGN FOR A WIRELESS DATA ACQUISITION DEVICE

An Honor Thesis

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By

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ABSTRACT

This report documents the design of an analog signal conditioning subsystem for a general purpose data acquisition device. The method of differential inputs is used to better control the common noise in input signals. The application flexibility of the device is maximized by combining amplifiers with selectable and wide range of gains, and variable filter cutoff frequency. Finally, test procedures and results are discussed and analysis the performance by comparing to the ideal design.

The analog signal conditioning is part of a larger collaborative effort involving several students during the 2004-2005 academic years. Therefore, the data acquisition goals and system requirements are reviewed to provide context for this work.

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1. Introduction

In recent years, wireless data acquisition devices are widely used in industry and academia. The application of data acquisition devices ranges from monitoring temperatures, vehicle movements, to security surveillance [1][2]. As the demand for data collection increased, the number of companies manufacturing relative products also multiplied. However, current products are costly, offer little flexibility in signal conditioning, and do not offer wireless control with large bandwidth. Further, few products offer high dynamic range and precision timing. Hence, the purpose of this project is to provide a low-cost data acquisition device that collects data from multiple sensors and transmits the data wirelessly.

The data acquisition device should be applicable to any type of sensor signals as well as multiple types of sensors to serve the goal of a general purpose data acquisition device. In order to sample multiple sensor signals, the device should have six or more channels with at least 16 bits of resolution after simultaneous sampling. All channels should reject common mode voltage in the input signals by implementing differential inputs. To better process various types of sensor signals, the device should have controllable gains in the range of 0dB to 60dB with variable filter cutoff frequency. Furthermore, the data transfer and power supply need to be provided through universal serial bus (USB) connection which allows high data transfer rate with 5V supply voltage. The sampling rate should exceed 8 kHz to record signals with frequencies up to 4 kHz without aliasing. Finally, the sampled data should be wirelessly transferred to a host computer using IEEE802.11 standard [3].

For the scope of this thesis, the main focus will be conditioning analog sensor signals for analog-to-digital conversion. The analog signal processes are compromised of amplifying the sensor signals to fully cover the input range of analog-to-digital converter (ADC) and eliminating unnecessary noise with an anti-aliasing filter. The full use of ADC input range minimizes quantization error from sampling, and the low pass filter removes undesired frequency components in the collected signals.

In this research project, the main focus is on designing an analog signal conditioning system that is applicable to any type of sensor. We start with a brief explanation of the concept of differential amplification. Then, we present the overall structural design of the system as well as the detailed design approach of the subcomponents. Then, we introduce experimental procedures used to test our design. Finally, test results are analyzed and verified against the initial design goals.

2. The Concept of Single Ended and Differential Amplification

Differential amplification is known as magnifying the voltage difference between non-inverting and inverting inputs of an operational amplifier. The merit of using differential amplification is that the input configuration optimizes data acquisition system performance by eliminating the common mode voltage and prevents possible hardware damage [4].

The common mode voltage (CMV) is an in-phase signal that appears simultaneously on both input terminals of a data acquisition channel. The effect of CMV on data acquisition device is that CMV may offset the signal beyond the measurement range of ADC or may exceed the maximum overvoltage rating of the data acquisition

front end, possibly putting the operator and the hardware at risk [4]. The presence of CMV in the input of data acquisition device is shown in Figure 2.1.

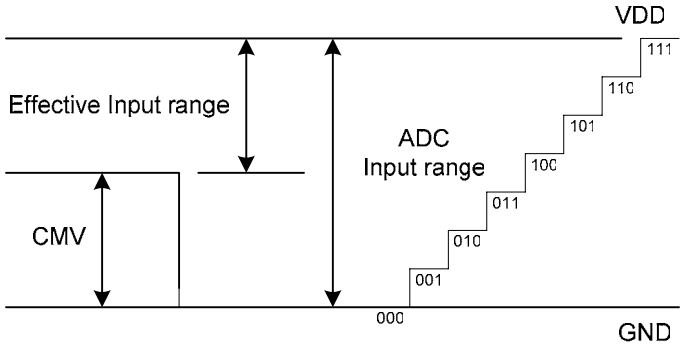

Figure 2.1: Effect of CMV on Input Range

The input range of analog-to-digital conversion is confined by the supply voltage (VDD) and the ground (GND). As shown in Figure 2.1, it is rather clear to find the effective input range in the presence of CMV.

$$Effective\_Input\_Range = VDD - GND - CMV \quad (1)$$

For instance, if we assume 3 bit analog-to-digital conversion as shown in Figure 2.1, the presence of CMV reduces the effective input range to half of the initial scale. This decreases in effective resolution of ADC to 2 bits, thereby doubling the quantization error relative to the input signal. Therefore, rejecting CMV before analog –to-digital conversion is critical to maximize the performance in data collection.

The maximum CMV of a data acquisition input is the difference between the signal of interest and the full scale measurement of the input. Depending on the magnitude of CMV relative to the input range of the ADC, the measurement applications are divided into single-ended, differential input, and isolation.

The difference between the single-ended and differential input is that for single-ended, the low signal input is connected to the common ground. On the other hand, for the application of differential input, the actual input is the difference of the two input signals. When no CMV exists in the input signals, signal ended is implemented. However, when CMV is present, single-ended amplifies the CMV whereas differential input rejects any CMV and measures balanced inputs. This is clearly shown in Figure 2.2.

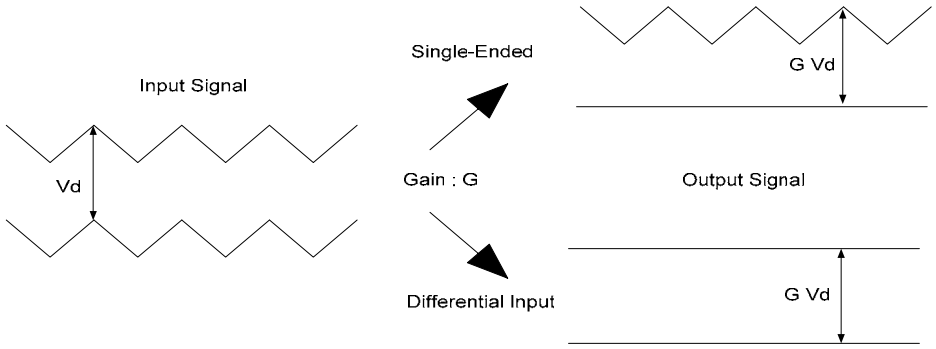

Figure 2.2: Single-Ended vs. Differential Input in the Presence of CMV

In digital signal processing applications, additive noise typically contribute to CMV; therefore, applying differential input is usually a better choice than single-ended.

However, there is a limitation to the differential input. In the case where CMV exceeds the full scale of the ADC, the overvoltage can damage the analog front of the data acquisition device. To prevent this from happening, isolation circuit is attached to prohibit high current flowing into the analog front end. However, due to the increased complexity in the input configuration, the isolation scheme is omitted in our design [4].

For our design, all channels are equipped with differential inputs to remove possible CMV that might be present in the sensor signals. The detailed design specifications will be discussed after the system design overview.

3. Overall System Structure

The overall system block diagram is shown in Figure 3.1. The entire system can be divided into four subsystems: Analog signal conditioning system, ADC, Microcontroller, and a host computer. The analog signal conditioning system consists of differential amplifiers, second stage amplifiers, and anti-aliasing filters. Four inputs signals are available for any type of sensor connection. The four inputs are VDD, V+, V-, and GND. V+ represents non-inverting input of the differential amplifier whereas V- corresponds to inverting one. Then, the processed signals are sampled by Texas Instrument ADS8364 ADC [6] which allows simultaneous sampling of six channels. The ADC sampling is controlled by Cypress AN2131[7] and the sampled data is transferred to the microcontroller 8 bits per cycle. Then, the data is transferred to a Single Board Computer (TS-7200) through a USB connection [8]. The Single Board Computer either transmits the collected data wirelessly to a Master Computer or stores the data on the embedded compact flash card. Negated End Of Conversation(EOC-) bit from the ADC is linked to the Single Board Computer to provide precision timing information [6]. The microcontroller controls second stage amplifiers and anti-alias filter cutoff frequency with a total of 11 I/O pins for all six channels. The microcontroller, ADC, and signal conditioning operates on 3.3V which is available from the USB after voltage regulation.

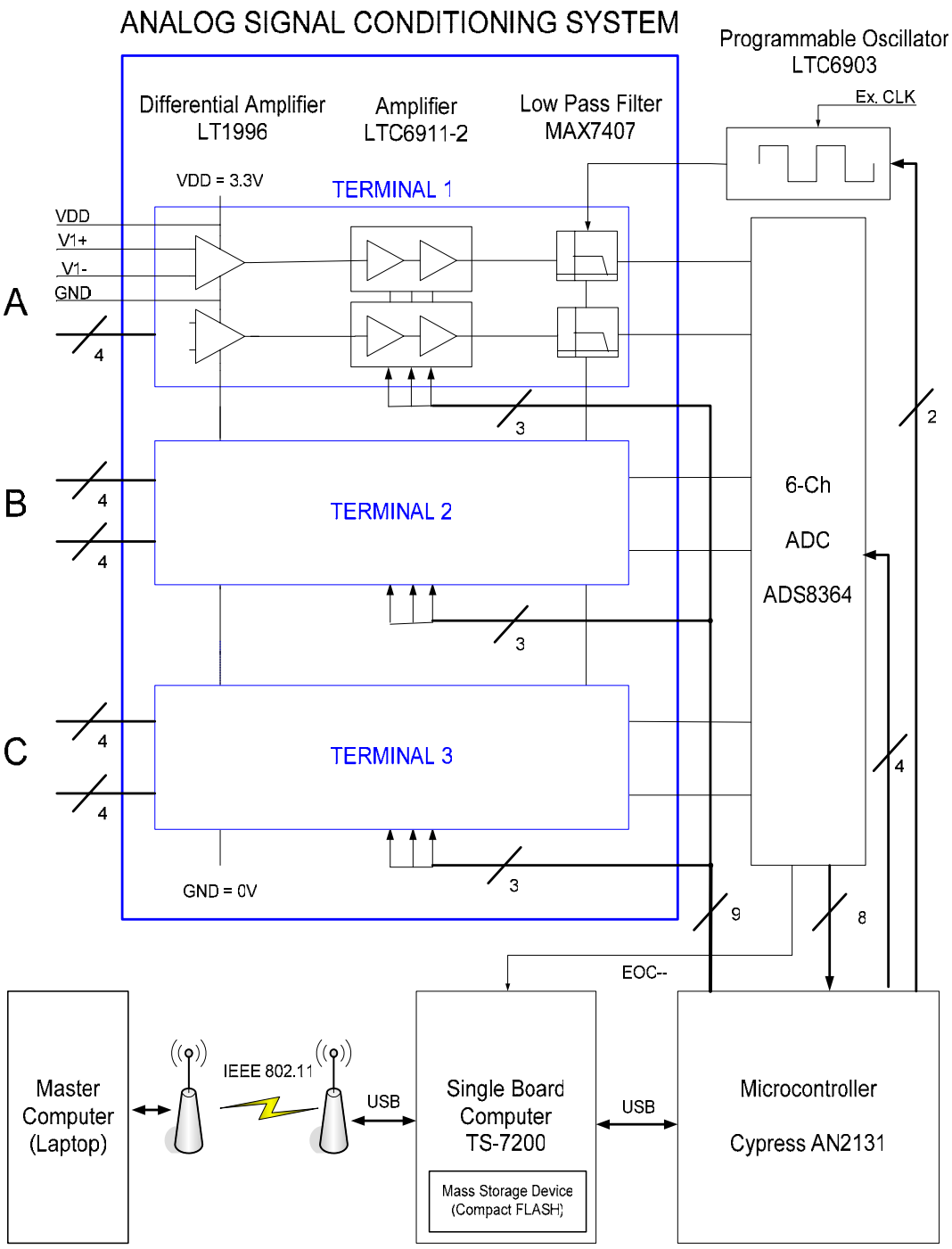

Figure 3.1: System Block Diagram

4. Analog Signal Conditioning System

For the analog signal conditioning, each channel should consist of three main stages: differential amplification, dual amplification, and anti-aliasing filtering. The differential amplifier magnifies the difference in two input voltages with a set gain of 2.98V/V. Then, the signals are further amplified to the range that fully covers the input scale of ADC. Finally, the noise is filtered by a low pass filter with a cutoff frequency smaller than the half of sampling frequency. This condition satisfies the Nyquist theorem and hence, prevents aliasing.

The product selections of the subcomponents were based on several factors. In the case of the differential amplifier, simple circuit implementation is required. The total number of available input/output pins of Cypress microcontroller [7] is limited, and no additional pin is available for varying differential amplification. In the case of the amplifier, a wide range of gain factors is needed in order to accommodate sensor signals with very low voltages. Furthermore, the gain pins must be controlled digitally which allows user to define the gain before starting the data collection. Lastly, to fulfill 16 bit sampling resolution, -96dB attenuation of noise is required. Therefore, the specifications of a low pass filter are a minimum filter order of 8 and attenuation greater than -96dB in the stopband. The attenuation factor is based on assuming -6dB attenuation per resolution bit and total of -96dB attenuation is required for 16bit resolution. The componets that meet all the specifications are introduced in Table 1.

Table 1: Analog Subcomponent Specifications

Subcomponents	Manufacturer	Model No.	Specifications
Differential Amplifier	Linear Technology[5]	LT1996	Differential amplifier with selectable gains
Amplifier	Linear Technology[9]	LTC6911-2	Dual matched amplifiers with digitally programmable gains
Anti-aliasing Low Pass Filter	Maxim Semiconductor[10]	MAX7407	8^{th} order Elliptic filter with clock tunable cutoff frequency
Programmable Oscillator	Linear Technology [11]	LTC6903	1kHz – 68MHz Serial Port Programmable Oscillator

There are six channels which are grouped as three terminals of two channels each, as marked in alphabetical order in Figure 3.1. The dual channels that are in the same terminal share common control pins for the amplifiers. However, the cutoff frequencies of low pass filters are uniform since the sampling rate is the same for all channels. Division of six channels into three terminals of two channels each with the uniform gain per terminal allows simultaneous data collection of three different types of sensors.

All channels are built to provide four types of inputs: VDD, V+, V-, and GND. VDD and GND are provided as inputs to supply 3.3V operating voltage to the sensor circuit if needed. However, the actual input connections are established by wiring sensor

circuit to the inverting (V-) and non-inverting inputs (V+) of the LT1996 differential amplifier [5].

The cutoff frequencies of the filters are determined by the input clock frequency. The set ratio between the input clock frequency to the cutoff frequency is 100 to 1. The input clock of the filter is generated from a serial programmable oscillator by LTC6903 [11]. The variable oscillator requires two control lines from the microcontroller: Serial Data Input (SDI) pin receives serial data for setting the oscillation frequency and Serial Port Enable (SPE) initiates serial transaction when brought low. The oscillator connection to the external clock is also necessary. The same external oscillator used for the microcontroller can also be applied to the programmable oscillator.

4.1 Differential Amplifier

The connection of differential amplifier configured to have a set gain of 2.89V/V. The LT1996 combines a precision operational amplifier with eight precision resistors to from a one-chip solution for accurate amplifying voltages. The device is particularly well suited for use as a difference amplifier, where the precise resistor matching results in a common mode rejection ratio of greater than 80dB. The internal circuit and pin assignments are shown in Figure 4.1 [5].

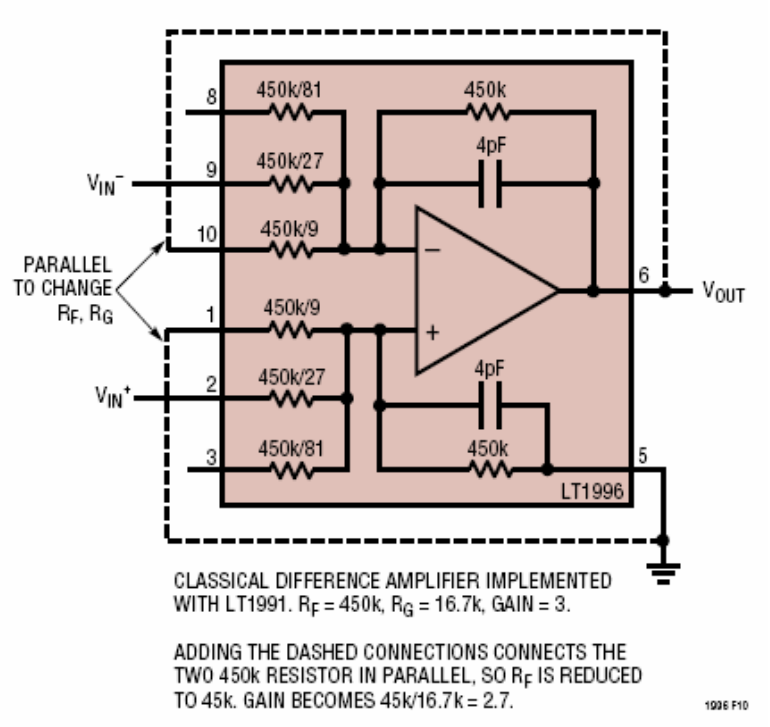

Figure 4.1: Internal Circuit Diagram of LT1996 [5]

For single supply voltage, the differential amplifier requires voltage reference (Vref) pin biased at the midpoint of 3.3V supply voltage. Since LTC6911-2 has Vref that internally sets the pin to 1.65V, the Vref pins of the differential amplifier and second stage amplifier are shorted. The implemented schematic diagram is shown in Figure 4.2. The bridge capacitor might reject very low frequencies. This will be verified when tested.

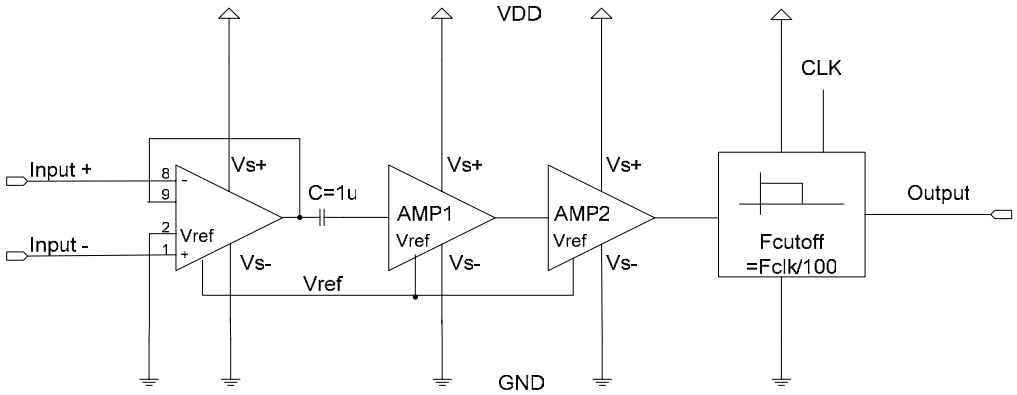

Figure 4.2: Schematic of Analog Signal Conditioning System

4.2 Digitally Selectable Gain Amplifier

The LTC6911-2 is a family of low noise digitally programmable gain amplifiers that are simple to use. The matched gain of both channels is adjustable using a 3-bit parallel interface to select voltage gains of 0, 1, 2, 4, 8, 16, 32, and 64V/V. A half-supply reference generated internally at the AGND pin. The single LTC6911-2 Integrated Chip by Linear Technology has two channels with dual amplifiers. The gain of both amplifiers are set by highs and lows on three control pins. Using two amplifiers with two different signals creates too much cross-interference noise between the two channels. The internal circuitry and single supply configuration are shown in Figure 4.3 [9].

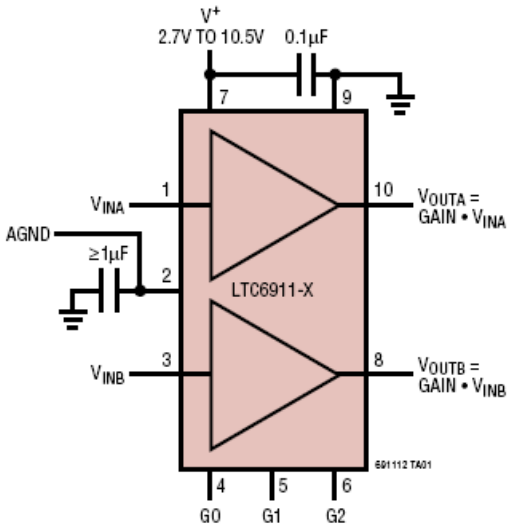

Figure 4.3: LTC6911-2 Internal Circuitry and Single Supply Configuration [9]

To eliminate the cross-interference and maximize the usage of amplifiers, the design decision has been made to double amplify a single channel on a single chip. In other words, the output of one amplifier is directly routed to the input of the second amplifier on the same chip as shown in the Figure 4.1. By implementing double

amplification on a single channel, the available gain factors with corresponding control pins are as listed in Table 2. Note that the differential amplifier has a set gain of 2.89V/V.

Table 2: Variable Gain Factors after Double Amplification

Digital Inputs			Gain in V/V
G2	G1	G0	LTC6911-2
0	0	0	0
0	0	1	2.89
0	1	0	11.56
0	1	1	46.24
1	0	0	184.96
1	0	1	739.84
1	1	0	2959.36
1	1	1	11837.44

4.3 Tunable Low Pass Filter

The MAX7407 is an 8^{th} order lowpass Elliptic Filter with low noise and distortion. The device draws 2mA of supply current and allows corner frequencies from 1Hz to 10kHz. Two clocking options are available: self-clocking (through the use of an external capacitor), and external clocking. For better control of cutoff frequency, we decided to clock the filter with an external oscillator. The ratio of clock frequency to the cutoff frequency is 100 to 1. The typical operating circuit of MAX7407 is shown in Figure 4.4 [10].

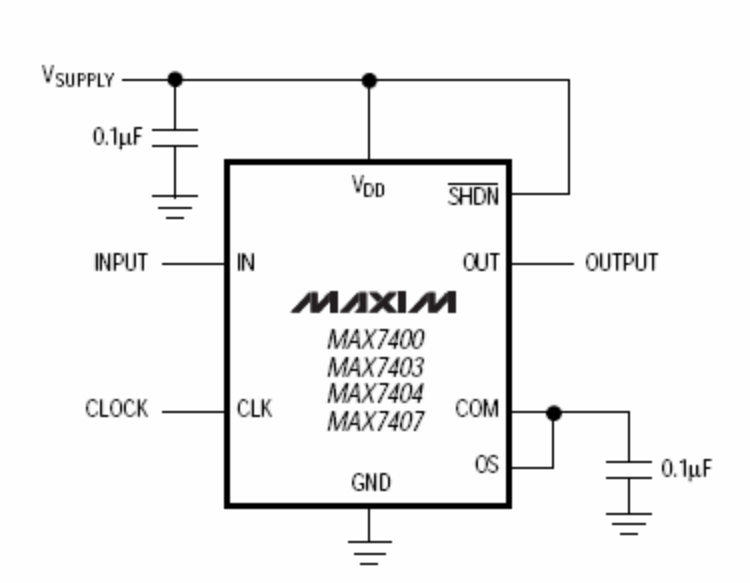

Figure 4.4: Operating Circuit of MAX7407 [10]

The programmable oscillator is capable of generating a clock frequency from 1 kHz to 68 MHz. The allowable range of cutoff frequency is from 1Hz to 10 kHz. Thus connecting the two permits the actual cutoff frequency to be between 10 Hz and 10 kHz.

Two control pins are used for serially programming the oscillator. The control lines are Serial Port Enable (SEN) and Serial Data Input (SDI). SEN initiates serial transaction when brought LOW. Then, during the next 16 clock cycles, 16 bits of serial data is read through SDI. After 16 cycles, SEN is brought high marking the end of configuration. The timing diagram is shown in Figure 4.5 [11].

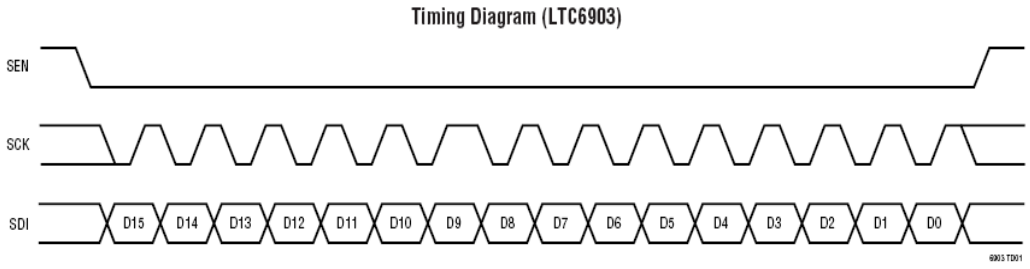

Figure 4.5: Timing Diagram of LTC6903 [11]

5. Tests and Results

5.1 Functionality Test

The functionality test is separated into two distinct signal processing steps: amplification and filtering. Tests are conducted with signals produced by a function generator.

Before testing the entire analog signal conditioning system, individual components are tested to ensure proper operation of each component. Figure 5.1 plot shows the magnitude response of the low pass filter in a linear scale and the low frequency region is zoomed in Figure 5.2. The filter test shows 1 kHz cutoff frequency which equals to one hundredth of the input clock frequency [10]. The peak-to-peak input voltage was set to 500mV, but the function generator used for testing is unable to generate sinusoid with full 500mV magnitude up to 5Hz.

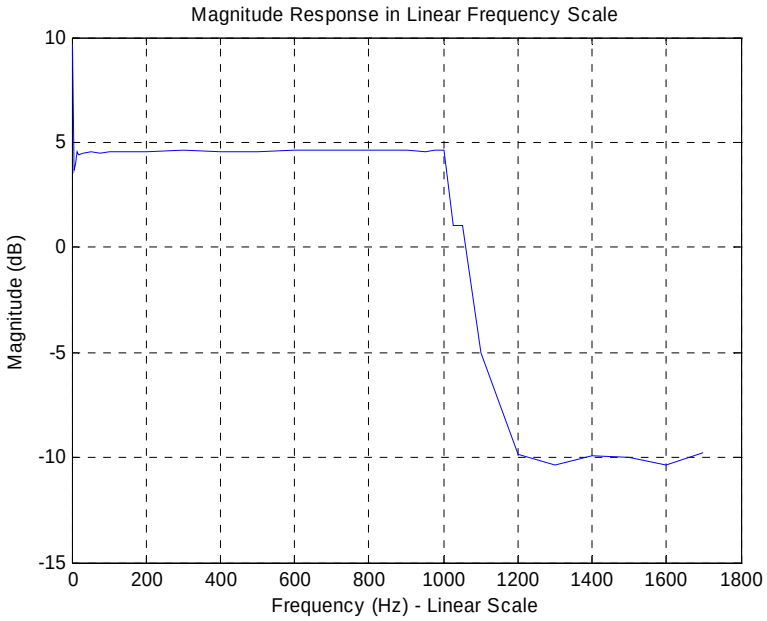

Figure 5. 1: Magnitude Response of Anti-aliasing Filter

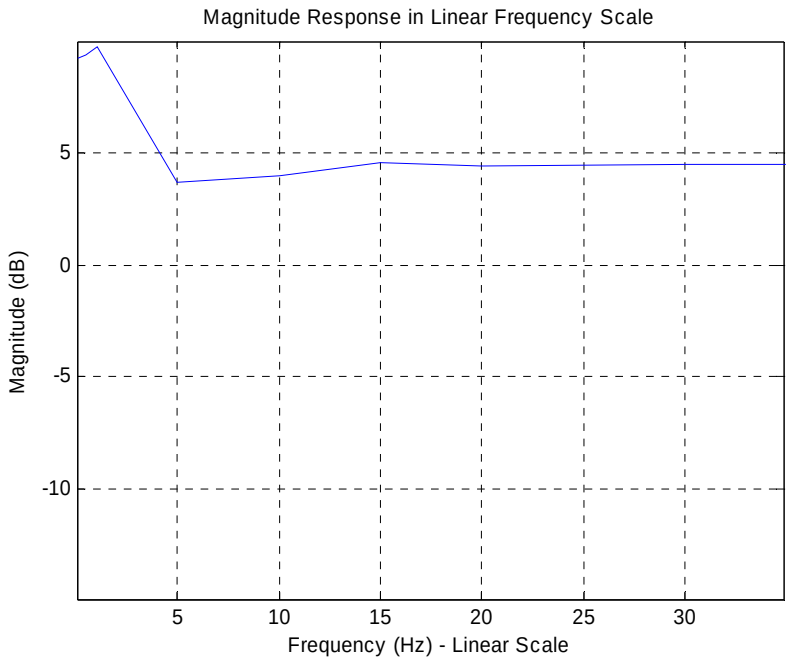

Figure 5. 2: Low Frequency Magnitude Response of Anti-Aliasing Filter

The passband at very low frequency stabilizes after 5Hz. The passband has a set DC gain of 2.89V/V which is the fixed offset of the differential amplifier. The low frequency distortion is caused by the presence of the bridge capacitor between the differential amplifier and the second stage amplifiers. However, due to precision limitation of function generator and accuracy of our oscilloscope, high gain occurs up to 5Hz as shown in the Figure 5.2.

Next, the amplification of the analog system is tested. The differential amplifier has a set gain of 2.89 V/V and the second stage gain factors were tested using the LTC6911-1 gain factors 1, 4, 25, 100, 400, 2500, and 10,000. The graph is shown in Figure 5.3.

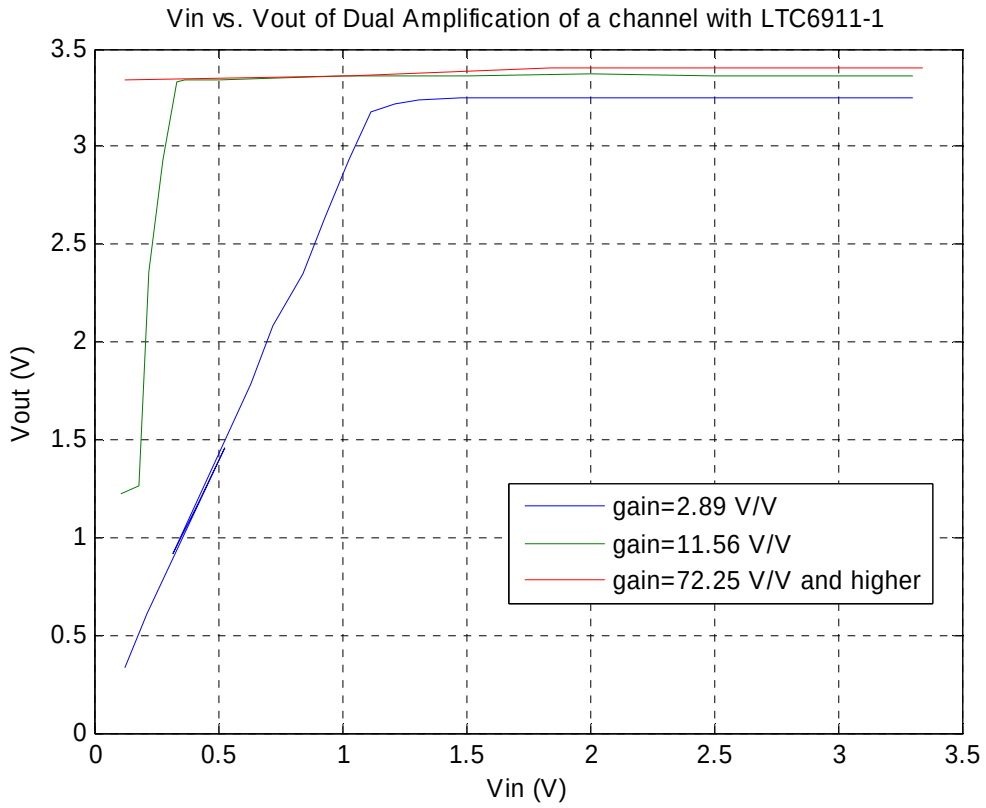

Figure 5.3: Vin vs Vout of Differential and Second Stage Amplification

We were unable to apply input voltages smaller than 100mV with our function generator. The gain factor of 72.25 and higher cause the input voltage to saturate which is represented as a flat line in the Figure 5.3.

To evaluate performance analysis, two points are chosen in the graph and the calculated slope is compared to the actual gains.

For the case of 2.89 V/V gain, the slope from the point (0.1791, 0.5), to the point (1,2.853) is

$$slope\_by\_calculation = \frac{y_2 - y_1}{x_2 - x_1} = \frac{2.853 - 0.5}{1 - 0.1791} = 2.866\frac{V}{V}$$

$$Percentage\_of\_error = \frac{\left| true\_gain - computed\_gain \right|}{true\_gain} = \frac{\left|2.89 - 2.866\right|}{2.89} \times 100 = 0.83\%$$

Similarly, for the case of 11.59V/V gain, the slope from the point (0.1904, 1.5) to (0.2859, 3) is

$$slope\_by\_calculation = \frac{3 - 1.5}{0.2859 - 0.1904} = 15.71$$

$$Percentage\_of\_error = \frac{\left|15.71 - 11.59\right|}{11.59} = 35.5\%$$

For the gains greater and equal to 72.25, it has no meaning to calculate the slope since all measure voltages are saturated.

5.2 Acoustic Signal Test

The entire analog signal conditioning system is tested with a pair of microphones on breadboard. The picture of breadboard prototype is shown in Appendix B. The biasing circuit used in the test are shown in Figure 5.4. The input connections use three of four available lines. The microphone circuit is shown in Figure 5.4.

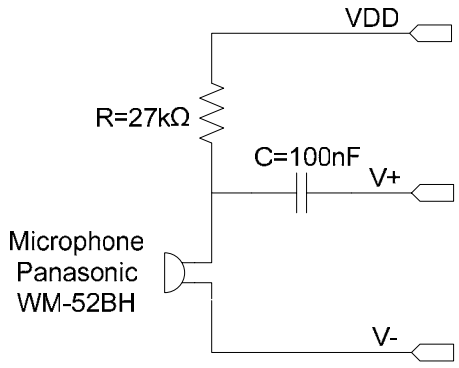

Figure 5.4: Biased Circuit for Microphone [12]

For this test case, both amplifier gains and filter cutoff frequencies are set to observe the same signals with different gains and cutoff frequencies. The results are displayed on an oscilloscope. Since two channels with identical microphones are tested with the same sound source, only difference in the output signals is the signal conditioning factor.

Figure 5.5 shows the filtered output tested with the same sound source generated by playing music. The only difference between the two channels is the cutoff frequency. The top waveform is generated with 1 kHz filter cutoff frequency and the bottom graph is filtered at 6kHz cutoff frequency. Clearly, the high frequency component in the bottom waveform is effectively eliminated in the top waveform.

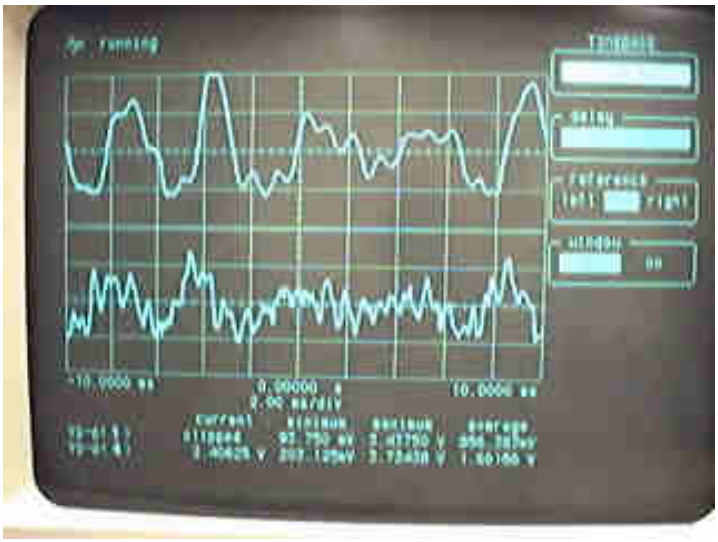

Figure 5. 5: Acoustic Signal Testing with cutoff frequencies of 1 kHz (Top) and 6 kHz (bottom)

On the other hand, test results of two channels with the same cutoff frequency, but different gains are shown in Figure 5.6. The waveform on the top has been amplified by a gain of 72.25, whereas the bottom by a gain of 289. The curves of the waveform on the

top are not easy to recognize whereas the bottom clearly distinguishes peaks and valleys of the waveform. The peak to peak voltage of the top waveform is 283mV and the bottom one is 1.373V.

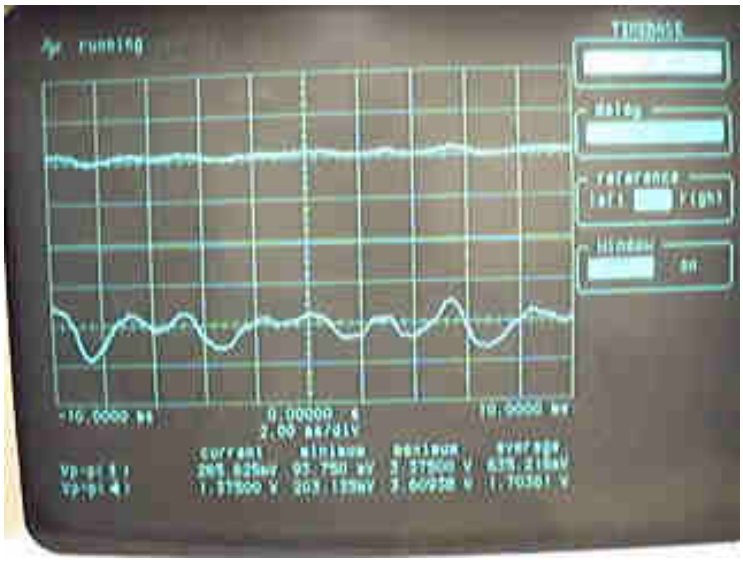

Figure 5. 6: Acoustic Signal Test with the gain of 72.25(top) and 289(bottom)

6. Conclusion

The intended goal of this project was to build an analog signal conditioning system that features differential inputs with selectable gains and variable filter cutoff frequencies for a general purpose data acquisition device. Major design upgrades have been made from the first version of signal conditioning system which had a fixed cutoff frequency and single-ended inputs that are vulnerable to CMV.

In the performance point of view, the updated general purpose analog conditioning system is able to sample data with full 16 bits resolution in the presence of CMV. Therefore, the new system can be used in industrial or research applications where both accurate data collection and noise elimination are needed. Furthermore, the breadboard prototype fulfills all the specifications set at the start of this project.

The remaining tasks for this project are to create a board layout for printed circuit board prototypes and test the prototypes. After successfully passing these stages, the product will provide low cost data collection.

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Appendix A: Tutorials: Designing Printed Circuit Board using Eagle

For designing a Printed Circuit(PC) board layout, Eagle 4.13r1 software released by CadSoft Online was used. There are two routes to completing a board layout. One is to design a schematic and convert it to a board layout and the other is to create a board layout by directly placing components on a board layout. The first approach was taken since it is easy to make changes in schematics which corresponding change occurs in the board layout. Also, most of the work needed to transfer a schematic to a board layout is done by the software itself.

The components that are added to schematics and boards are stored in libraries. The Library Editor allows users to create a library file of a component that consists of a package, symbol and device representations. The package represents a foot print in the layout and the symbol represents drawing for a schematic. Lastly, the device represents a real component, consisting of symbols and packages.

The initial task of designing a board layout started with creating libraries for LTC6911 and LTC1563 which is not included in a free bundle. First, the package representation is designed by drawing chips according to their actual physical dimensions shown in the data sheets. The specific details of designing a package representation are illustrated in the Eagle Tutorial. Next, the symbol representation is completed by drawing a box with attached pins labeled accordingly. The name and value of the component are also included. The symbol of a component is the schematic view which only needs to represent key elements such as pins, name and value of the component. Further information of the chip can be added if needed. As part of the symbol representation, a description of the component needs to be specified which is used for keyword search.

Lastly, the device representation is constructed by including additional data to the symbol representation. Both LTC1563 and LTC6911 libraries were created and added to the default Linear-Technology library. Figure A.1 and Figure A.2 show the library representations of LTC1563 and LTC6911, respectively.

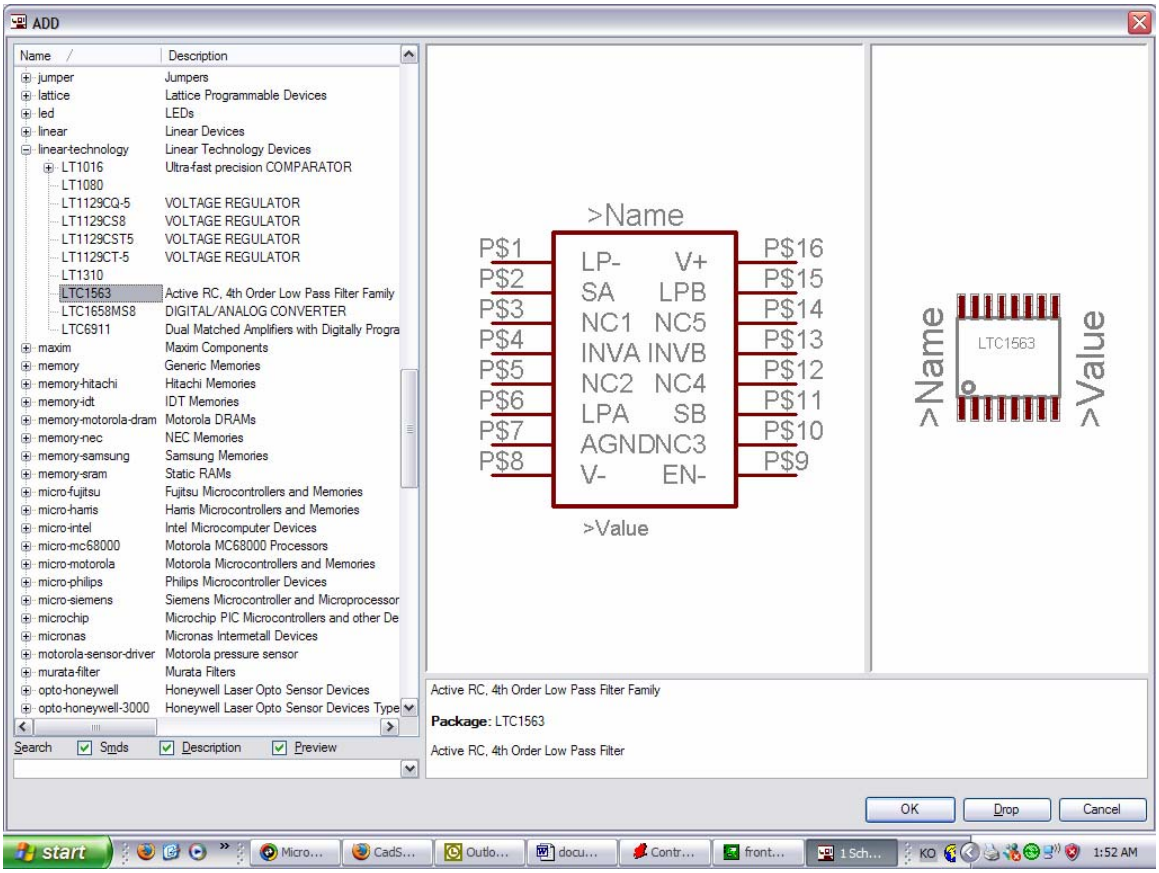

Figure A.6: LTC1563 Library Design

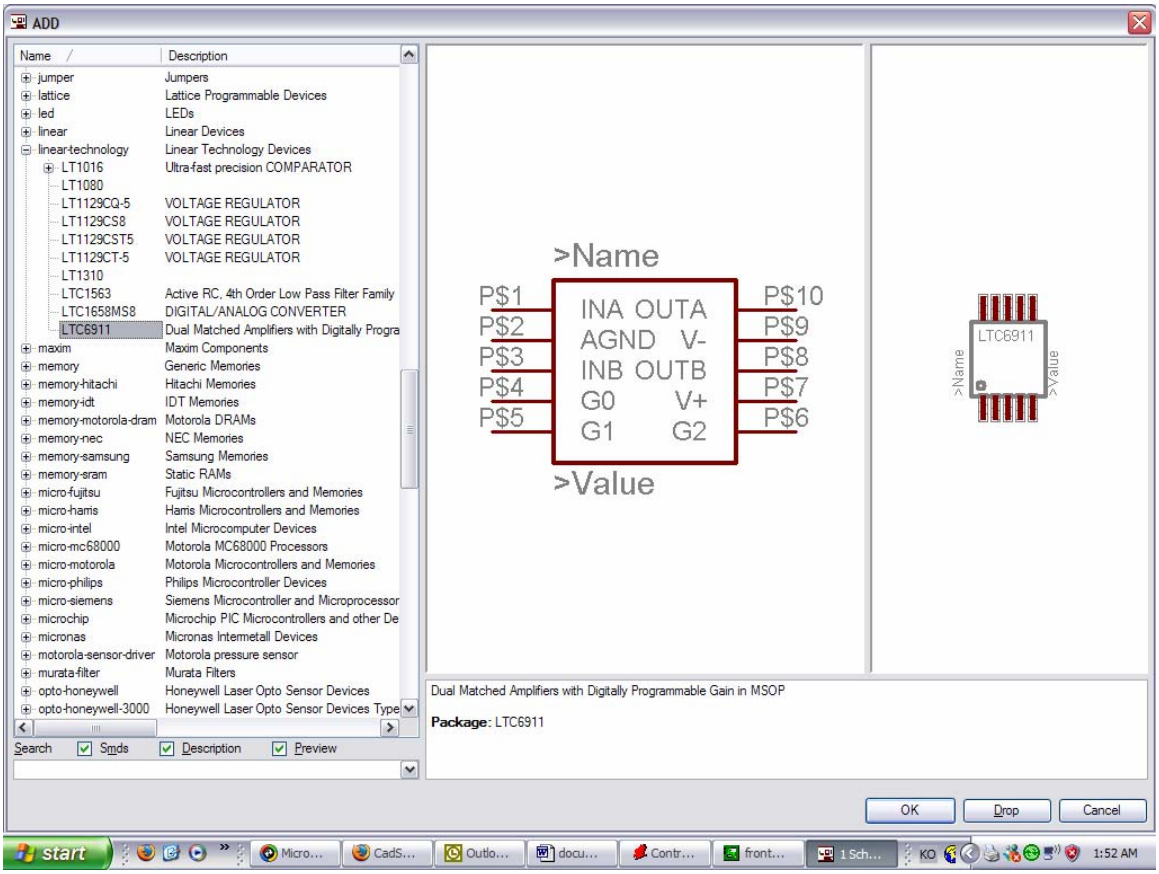

Figure A.2: LTC6911 Library Design

Once all library representation of every component that will be used in the design schematic is prepared, the following step is to create a schematic. The process of generating a schematic is a straight forward: add all symbols of components in a schematic, wire up all the components, and specify name and value of components if needed. Figure A.3 shows the schematic drawing of the front end. For supply voltage, ground, microphone and amplifier control pin connections, pin headers are used to establish direct physical connection.

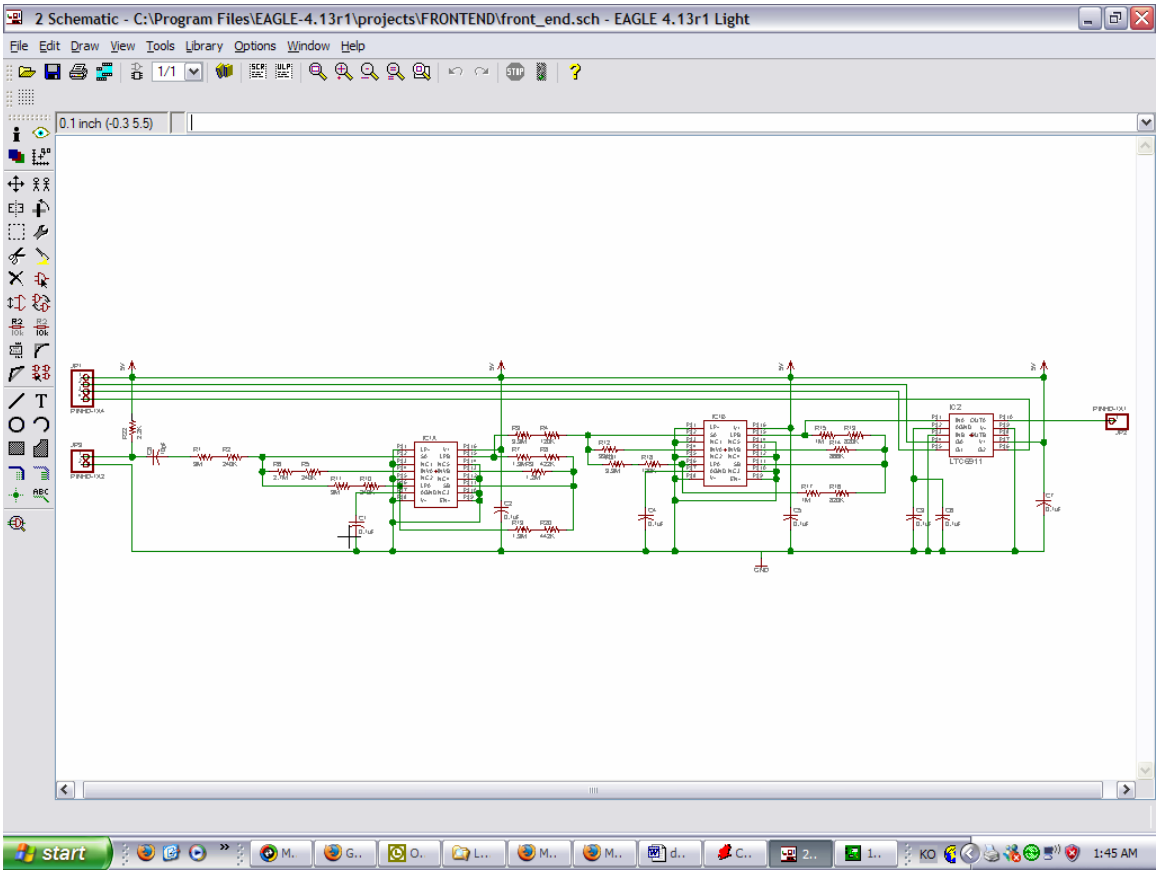

Figure A.3: The Front End Schematic

Converting a schematic to a PC board layout is another simple process. By implementing 'Board' function of the schematic editor, the eagle software automatically transfers all components in the schematic to a new board editor window. On the left side of the window, components are connected with 'airwires' which is the temporary representation of connections. On the right side of the window, the actual board boundary is shown which can be manually adjusted. Users need to drag and drop every component into the boundary. Only supply voltage and ground connections are manually routed and all the other connections are implemented by 'Auto' routing function of the board editor. The software automatically converts airwires into physical connections by finding the shortest routes and preventing wire overlaps. Figure A.4 represents the PC board layout of the front end design.

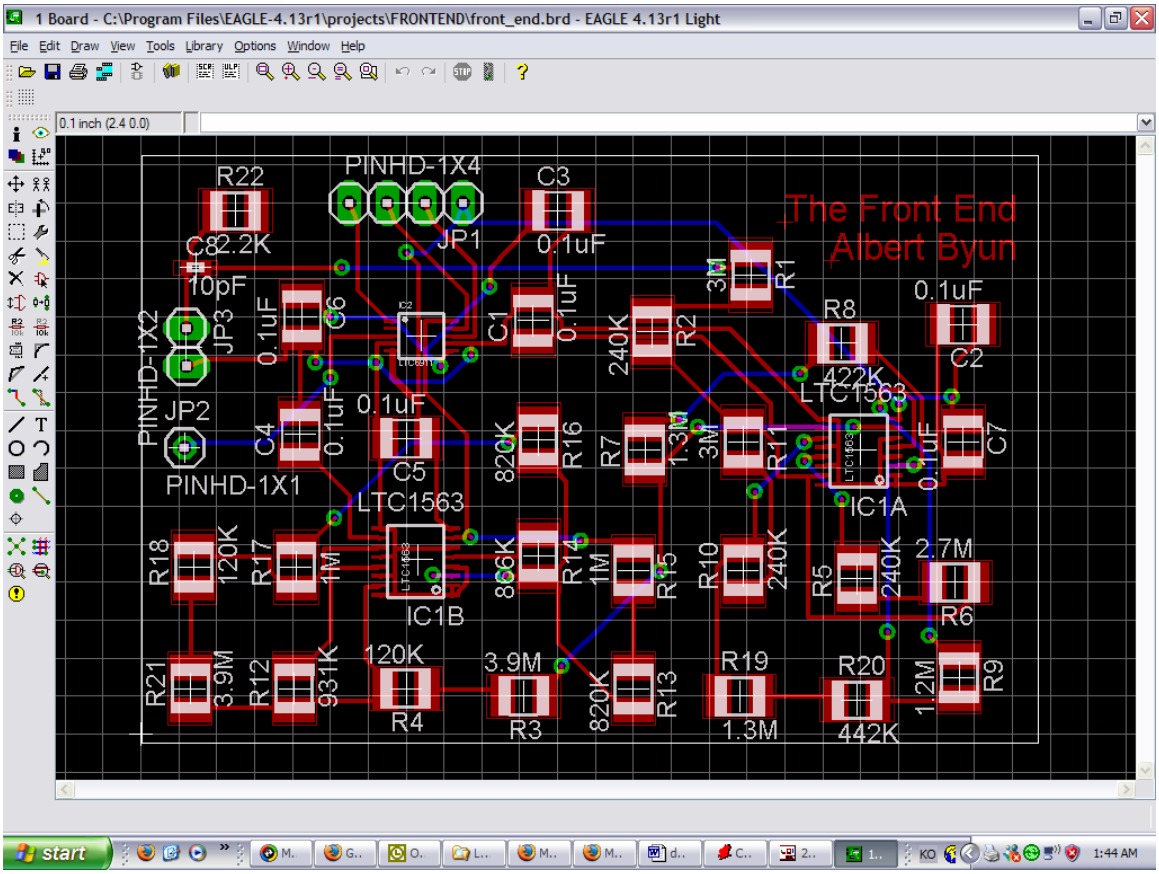

Figure A.4: The Front End Board Layout

One the most important aspect of creating a board layout is the placement of components into the board boundary. As mentioned in the previous paragraph, this process is manually controlled. By rotating the components and grouping together those components that are connected to the same chip, users are able to find ultimate component locations that results in minimum board space usage.

Appendix B: The Complete Breadboard Prototype