Maximizing Digitizer Dynamic Range

Agilent Technologies

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Agenda

1. Introduction
   Identifying a digitizer application
   Block diagram overview

2. Dynamic range limitations
   Analog to digital converter (ADC)
   Front-end amplifier (FEA)
   Clocking and synchronization

3. Increasing Dynamic Range
   Channel stacking

4. Agilent State-Of-The-Art High Dynamic Range Digitizer
   High-Speed Digitizer Technology Expertise
   AXIe 12-Bit High-Speed Digitizer – See events that you could not see before
Typical Experiment or Measurement

Large amounts of data are converted into images and maps

Host processor for control and data analysis

Agilent Digitizer converts the analog electrical signal to digital information

Generate a stimulus (laser) which could be ultrasound or radio waves in other app’s

Capture pulses with a sensor, an optical-electric converter or in other app’s antenna or transducer

Size/power, speed, accuracy & lower cost of ownership

Phenomena, Interaction or Event
Achieving Single-Shot Acquisitions

Installing Required Channels
- Integrate into 2, 5 or 14 slot chassis
- Synchronize >80 ch

System Synchronization
- Backplane local bus
- External clocking schemes
- Trigger time interpolation

Accurate Measurement
- Beyond banner specs
- Taking all sources of error into account

Data Storage
- Large memories
- Data recording
- Battery backup

Operational Software
- Management of system configuration
- Data acquisition safety
- Fail-safe operation

ENOBS
SINAD
SNR
THD
Thermal Noise
....
Simplified One-Channel Digitizer Architecture

Glossary of Acronyms:

- **FEA** – Front-end Amplifier
- **ADC** – Analog to Digital Converter
- **FPGA** – Field Programmable Gate Array
- **DDR** – Double Data Rate
- **SDRAM** – Synchronous Dynamic Random Access Memory

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Agilent High-Speed Digitizer
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ADC – Analog to Digital Converter

- Ideal ADC
  - Input is quantized into uniform steps
  - Transitions at +/- 50% of Δ
  - Discretely spaced samples at an infinite sampling rate
- ADCs have their own errors/performance
  - Offset/gain error
  - INL/DNL
  - ENOB, SNR, SFDR
  - …
- Digitizer design needs to maximize ADC performance
FEA – Front-end Amplifier

• Banner specifications
  - Offset range (example: +/-2*FSR)
  - Full scale range (example: 1V, 2V, etc.)
  - Input impedance (50Ω / 1MΩ)
  - Input coupling options (DC/AC)
  - 3dB analog bandwidth
  - Bandwidth limit filter (BWL)
  - Frequency response flatness (e.g. +/-1 dB)

• Design challenges – Sources of error
  - Reach wide bandwidth with DC coupling and high dynamic range
  - Large input DC offset
  - Good circuit protection
  - Whilst limiting the addition of noise and distortion
FEA – Challenges

• Reach wide bandwidth with DC coupling and high dynamic range
  - ADC inputs are usually differential, while digitizer inputs need to be single-ended → Requires a single-to-differential circuit
  - Single-to-differential circuit is usually either
    a) BALUN → No distortion added
    → Difficult to have DC coupling; bad DC to AC behavior
    → Can be quite high band
    b) Amplifier → Adds distortion
    → Easy DC coupling
    → Difficult to reach wideband

• Large input DC offset
• Good circuit protection
• All of that and still limiting the addition of noise and distortion
  - Components add thermal noise
  - Active components add distortion
Clock Creation and Distribution

- **Banner specifications:**
  - Added sampling jitter (example: 225 fs nominal)
  - Clock accuracy (example: ±1.5 ppm)
  - Clock modes (internal/external reference, etc)

- **Design Challenges:**
  - Minimize the added jitter to not deteriorate ADC performance
  - Distribute clocks precisely for synchronization across channels
  - Immunity to perturbations (high speed clocks)
Influence of Sampling Clock on Digitizer Performance

• ADC Maximum Reachable theoretical SNR (no distortion):

\[
ENOB = \frac{SINAD - 1.76}{6.02}
\]

\[
SINAD = \frac{S}{(N+D)} = \text{SNR, when no distortion}
\]

\[\rightarrow SNR_{\text{max}} = (\text{Resolution} \times 6.02) + 1.76\]

• Sampling jitter also limits the maximum reachable SNR in function of input signal frequency

\[
\text{NOISE}_{\text{min}} = -20\times\log(2\pi f \times \text{Jitter})
\]
How To Maximize Digitizer Dynamic Range?

• Increase ADC resolution
  - In the GHz area experiments traditionally use 8-bit ADCs with ENOB of approximately 6-7 Bits
  - State-of-the-art is now 12-bit → Design challenges are stronger!

• Processing techniques
  - E.g. averaging
  - Limited by sampling rate – again trade-off resolution/speed

• “Stacking” channels to increase the resolution
  - Requires very good channel-to-channel synchronization
  - Requires large DC offset ranges
Channel “Stacking”

- A pulse is launched through a precision 50 ohm splitter
- One path goes directly to an input channel
- The second path is attenuated. In this case the amplitude is reduced to 25% of the first path (-12dB). Use a more sensitive full-scale-range on Ch2 of the digitizer
- Change channel DC offset for “stacking” the channels → the input signal can be larger than a single window and the second channel will then record the over signal, and increase the number of quantization levels
Agilent High-Speed Digitizer Technology Expertise

High-Speed Digitizer design team:

- Best in class high-speed ADC implementation
- Small footprint and low power consumption
- High measurement throughput
- ASIC design, IP and technical know-how
- Multiple OS and software environment
- Advanced firmware development

A core of 300+ years of cumulative research and development experience in developing with ADC technology.
M9703A AXIe 12-Bit High-Speed Digitizer

See Events That You Could Not See Before!

Key Features
- 12 bit resolution
- 8 channels @ 1 GS/s or 1.6 GS/s (4 ch @ 3.2 GS/s when interleaved)
- Reach up to >100 phase-coherent channels
- DC to 2 GHz input frequency range
- DC to 1.4 GHz instantaneous BW
- Internal Customizable FPGAs
- 1.1 GB/s data transfer

M9703A OS support
- Windows
- XP (32-bit)
- Vista (32/64-bit)
- 7 (32/64-bit)
- Linux

Drivers – MD1 software
- IVI-C, IVI-COM
- LabVIEW
- Matlab (through IVI-COM)

OTS application software
- MD1 soft front panel
- AcqirisMAQS U1092A-S01/S02/S03
- 89600 VSA software
M9703A
See Things You Were Not Able To See Before!

- 4096 quantization levels per channel (12-bit ADC)
- Very high dynamic range at GHz frequency
  - >9 effective bits
  - Very low system noise level of <500 uV rms
- Versatile attributes and exceptional channel synchronization for high signal quality and a very large input window simultaneously
  - Precise offset control
  - Excellent timing and synchronization
  - Stacking: combined window is 8,192 levels → **13-bit resolution!!!**
## FRF Option Performance

<table>
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<th>Frequency</th>
<th>Standard</th>
<th>-FRF</th>
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<td>48 MHz</td>
<td>9.0 Typ</td>
<td>9.1 Typ</td>
</tr>
<tr>
<td></td>
<td>100 MHz</td>
<td>9.1 Typ</td>
<td>9.2 Typ</td>
</tr>
<tr>
<td></td>
<td>410 MHz</td>
<td>8.9 Typ (8.2 spec)</td>
<td>9.1 Typ</td>
</tr>
<tr>
<td></td>
<td>650 MHz</td>
<td>Not spec’ed</td>
<td>9.0 Typ</td>
</tr>
<tr>
<td></td>
<td>900 MHz</td>
<td>Not spec’ed</td>
<td>8.8 Typ</td>
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<tr>
<td>SNR</td>
<td>48 MHz</td>
<td>58 dB Typ</td>
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<td></td>
<td>410 MHz</td>
<td>56 dB Typ (54 dB spec)</td>
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<tr>
<td></td>
<td>650 MHz</td>
<td>Not spec’ed</td>
<td>57 dB Typ</td>
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<td></td>
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<td>55 dB Typ</td>
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<td>SFDR</td>
<td>48 MHz</td>
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<td>60 dBC Typ (52 dBC spec)</td>
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